4. (Twice Amended) A semiconductor integrated circuit according to claim 3, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

6. (Twice Amended) A semiconductor integrated circuit according to claim 5, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for a corresponding one of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

Please add new claims 8-17 as follows.

8. (New) A semiconductor integrated circuit comprising:

a sub reset signal generator, including at least one transistor having a threshold voltage, for generating a plurality of sub power-on reset signals on basis of the threshold voltage; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signals.

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9. (new) A semiconductor integrated circuit comprising:

a first sub reset signal generator, including a first transistor having a first threshold voltage, for generating a first sub power-on reset signal on basis of the first threshold voltage;

a second sub reset signal generator, including a second transistor having a second threshold value, for generating a second sub power-on reset signal on basis of the second threshold voltage; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of the first sub power-on reset signal and the second sub power-on reset signal.

10. (new) A semiconductor integrated circuit comprising:

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a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a plurality of pulse generators for generating pulses on basis of the plurality of sub power-on reset signals, respectively; and

a composite circuit for synthesizing the pulses to generate a main power-on reset signal.

11. (new) A method of initializing a semiconductor integrated circuit comprising the steps of: generating a plurality of sub power-on reset signals, each according to a threshold voltage of a transistor; generating a plurality of pulse signals as power-on reset signals, according to the plurality of sub power-on reset signals generated at timings different from each other; and initializing an internal circuit according to at least one of said power-on reset signals.

12. (new) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals, wherein said main reset signal generator includes:

a plurality of pulse generators for respectively generating pulses which are shorter than an interval between transition edges of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate said main power-on reset signal.

13. (new) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal.

14. (new) A semiconductor integrated circuit according to claim 13, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge which corresponds to one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

15. (new) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a reset terminal for receiving an external power-on reset signal supplied from the exterior of the semiconductor integrated circuit; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals and said external power-on reset signal.

16. (new) A semiconductor integrated circuit according to claim 15, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge which corresponds to one of said sub power-on reset signals and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

17. (new) A method of initializing a semiconductor integrated circuit comprising the steps of:

generating a plurality of power-on reset signals as pulse signals according to a plurality of sub power-on reset signals at timings different from each other, the pulse signals being shorter than an interval between transition edges of said sub power-on reset signals; and